ABSTRACT OF THE DISCLOSURE

An apparatus comprising a processor, an interface circuit and a memory. The processor may be configured to operate at a first data rate in response to a first clock signal. The interface circuit may be configured to (i) operate in response to the first clock signal, and (ii) convert data received from the processor over a system bus from the first data rate to a second data rate. The memory may be (i) coupled to the interface circuit and (ii) configured to present/receive data to/from the system bus at the second data rate.